WHAT IS CLAIMED IS:

1. An SDIO controller having a single-chip semiconductor device connecting a SDIO-compliant SDIO host device with a plurality of applications via an SD bus, comprising:

(a) an SD interface operably connectable with the SDIO host device to decode commands received from the SDIO host device, and to return a response to the SDIO host device;

(b) one or more application interfaces; and

(c) a temporary memory operably connected between the SD interface and the one or more application interfaces.

2. An SDIO controller according to claim 1, wherein the temporary memory comprises an R/W FIFO device.

3. An SDIO controller according to claim 2, wherein the one or more application interfaces are selected from the group consisting of a PCMCIA interface, a PC card bus interface, a UART interface, and a memory interface.

4. An SDIO controller according to claim 1, wherein the temporary memory in the SDIO controller comprises as many read memories as the number of application interfaces to temporarily hold data read out of SDIO applications; and at least one write memory operably connected to temporarily hold data to be sent out to the SDIO host.

5. An SDIO controller according to claim 4, wherein each read memory is a RFIFO device and the write memory is a WFIFO device.

6. An SDIO controller according to claim 1, wherein the temporary memory in the SDIO controller comprises at least one read memory operably connected to temporarily

hold data read out of SDIO applications; and at least one write memory operably connected to temporarily hold data to be sent out to the SDIO host.

7. An SDIO controller according to claim 6, wherein the read memory is a RFIFO device and the write memory is a WFIFO device.

8. An SDIO controller according to claim 2, further comprising a microcontroller unit for data control, wherein the microcontroller unit is connected to control the SD interface and the one or more application interfaces.

9. An SDIO controller according to claim 8, further comprising an I/O device connected to input and output control signals to and from the microcontroller unit.

10. An SDIO controller according to claim 9, wherein the I/O device is a general peripheral I/O device.

11. An SDIO controller according to claim 10, wherein the microcontroller unit operates to decode data when the data sent from the SDIO host device to the SDIO controller via the SD bus contains at least a register read/write address, a selected type of operation, a quantity of data, and arbitrary write data, and the microcontroller unit operates to access non-contiguous registers via an application interface.

12. An SDIO wireless communications card comprising:

(a) an SDIO controller comprising:

(i) an SD interface operably connectable with the SDIO host device to decode commands received from the SDIO host device, and to return a response to the SDIO host device;

(ii) one or more application interfaces; and

(iii) a temporary memory operably connected between the SD interface and

the one or more application interfaces;

(b) a wireless communications module operably connected to the SDIO controller via the one or more application interfaces; and

(c) an SDIO-compliant card enclosure, wherein the SDIO controller and the wireless communications module are disposed within the enclosure.

13. An SDIO wireless communications card according to claim 12, wherein the temporary memory comprises an R/W FIFO device.

14. An SDIO wireless communications card according to claim 13, wherein the SDIO controller further comprises a microcontroller unit for data control, wherein the microcontroller unit is operably connected to control the SD interface and the one or more application interfaces.

15. An SDIO wireless communications card according to claim 14, wherein the wireless communications module is selected from the group consisting of a IEEE 802.11b module, a IEEE 802.11a module, a IEEE 802.11e module, a IEEE 802.11g module, and a Bluetooth module.

16. An SDIO wireless communications card according to claim 15, further comprising one or more additional applications selected from the group consisting of a global positioning system and a personal handyphone system, wherein the one or more additional applications are operably connected to corresponding application interfaces of the SDIO controller.

17. An SDIO wireless communications module comprising:

(a) an SDIO controller comprising:

(i) an SD interface operably connectable with the SDIO host device to decode commands received from the SDIO host device, and to return a

response to the SDIO host device;

(ii) one or more application interfaces; and

(iii) a temporary memory operably connected between the SD interface and the one or more application interfaces; and

(b) a wireless communications module operably connected to the SDIO controller via the one application interface; wherein the SDIO controller and the wireless communications module are integrated on a single circuit chip to form the SDIO wireless communications module.

18. An SDIO wireless communications module according to claim 17, wherein the temporary memory comprises an R/W FIFO device.

19. An wireless communications card according to claim 18, wherein the SDIO controller further comprises a microcontroller unit for data control, wherein the microcontroller unit is operably connected to control the SD interface and the one or more application interfaces.

20. A method of transmitting write data from an SDIO host device to an SDIO application, the method comprising the steps of:

(a) connecting an SDIO application with an SDIO host device, wherein the SDIO application comprises an SDIO controller having an SD interface and an application interface;

(b) receiving a write command from the SDIO host device via the SD interface and interpreting the command;

(c) generating a command response signal using the SD interface and sending the command response signal to the SDIO host device;

(d) after the SDIO host device receives the command response signal, transmitting data from the host device to the SDIO controller via the SD interface, wherein the transmitted data includes at least a register read/write address, a selected

type of operation, a quantity of data, and arbitrary write data;

(e) decoding the transmitted data using a microcontroller unit of the SDIO controller; and

(f) accessing non-contiguous register addresses of SD memory in the SDIO application via the application interface by using the microcontroller unit so data sent from the SDIO host device is written into the SD memory of the SDIO application.